REMARKS

This is intended as a full and complete response to the Office Action dated April 2, 2009, having a shortened statutory period for response set to expire on July 2, 2009. Please reconsider the claims pending in the application for reasons discussed below.

Claims 1-12 are pending in the application. Claims 1-12 and 43-70 remain pending following entry of this response. Claims 1 and 5 have been amended. New claims 43-70 have been added to recite aspects of the invention. Applicant submits that the amendments and new claims do not introduce new matter.

Further, Applicants are not conceding in this application that those amended (or canceled) claims are not patentable over the art cited by the Examiner, as the present claim amendments and cancellations are only for facilitating expeditious prosecution of the claimed subject matter. Applicants respectfully reserve the right to pursue these (pre-amended or canceled claims) and other claims in one or more continuations and/or divisional patent applications.

Statement of Substance of Interview

On July 1st, 2009, a telephonic interview was held between Sanjay Shenoy, Applicant's Attorney and Examiner Midys Rojas. The parties discussed the cited references including *Dean* and *Hetherington*. Claim 1 was discussed. The parties also discussed proposed amendments to claim 1. The proposed amendments are reflected in this response.

During the interview, Applicant proposed amendments to the claims to recite an architecture wherein the processors and private caches, as claimed, are parts of a single processor module. The Examiner stated that the proposed amendments would likely overcome the cited art. However, the Examiner requested that a formal written response including Applicant's specific amendments and arguments be filed for further consideration.

Claim Rejections - 35 U.S.C. § 103

Claims 1-12 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over *Dean, et al.* U.S. Patent No. 6,604,174, in view of *Hetherington, et al.* U.S. Publication No. 2001/0010069.

The Examiner bears the initial burden of establishing a *prima facie* case of obviousness. See MPEP § 2141. Establishing a *prima facie* case of obviousness begins with first resolving the factual inquiries of *Graham v. John Deere Co.*, 383 U.S. 1 (1966). The factual inquiries are as follows:

(A) determining the scope and content of the prior art;

(B) ascertaining the differences between the claimed invention and the prior art;

(C) resolving the level of ordinary skill in the art; and

(D) considering any objective indicia of nonobviousness.

Once the *Graham* factual inquiries are resolved, the Examiner must determine whether the claimed invention would have been obvious to one of ordinary skill in the art.

Respectfully, Applicants submit that the cited references do not disclose all the elements of the claims, as amended herein.

For example, regarding claim 1, 5, and the claims that depend therefrom, the cited references do not disclose allocating cache lines from a first private cache associated with a first processor to a second processor based upon the difference between the cache miss rate for the first processor and the cache miss rate of the second processor, wherein a latency to access the allocated lines of the first private cache by the second processor is greater than a latency to access cache lines of a second private cache associated with the second processor, wherein the first private cache and the second private cache are at a same cache level, and wherein the processors and the private caches are parts of a single processor module.

Prior to the amendment made herein, claims 1 and 5 did not recite that the processors and the private caches are parts of a single processor module. The Examiner relied on the following lines of *Hetherington* to disclose that a latency to access the allocated lines of the first private cache by the second processor is greater than a latency to access cache lines of a second private cache associated with the second processor.

> Modern processors support multiple cache levels, most often two or three levels of cache. A level 1 cache (L1 cache) is usually an internal cache built onto the same monolithic IC as the processor itself. On-chip cache is the fastest (i.e., lowest latency) because it is accessed by the internal components of the processor. On the other hand, off-chip cache is an external cache of static random access memory (SRAM) chips plugged into a motherboard. Off-chip cache has much higher latency, although is typically much shorter latency than accesses to main memory. See *Hetherington*, Paragraph [0007].

As can be seen from in the paragraph above, *Hetherington* compares different latencies of an on-chip cache and an off-chip cache. However, the cited portions of *Hetherington* do not disclose anything about comparative latencies of private caches that are on the same processor module. Therefore, Applicant submits that the cited references do not disclose allocating cache lines from a first private cache associated with a first processor to a second processor based upon the difference between the cache miss rate for the first processor and the cache miss rate of the second processor, wherein a latency to access the allocated lines of the first private cache by the second processor is greater than a latency to access cache lines of a second private cache associated with the second processor, wherein the first private cache and the second private cache are at a same cache level, and wherein the processors and the private caches are parts of a single processor module.

Therefore, the claims are believed to be allowable, and allowance of the claims is respectfully requested.

Conclusion

Having addressed all issues set out in the office action, Applicant respectfully submits that the claims are in condition for allowance and respectfully requests that the claims be allowed.

Respectfully submitted, and
S-signed pursuant to 37 CFR 1.4,

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